WHAT IS CLAIMED IS:

1. An error correction device comprising: a buffer memory for storing at least one sector of data having a structure where each of N words of error correcting code comprises a data unit, an inner code parity unit, and one error detecting code; a syndrome calculating means for generating syndrome for data read from said buffer memory; an error correcting means for correcting error-containing data in said buffer memory by detecting an error position from the syndrome generated by said syndrome calculating means and by calculating an error value; an error detecting means for detecting an error, one sector at a time, in error-corrected data generated by said error correcting means; a storing means for storing mid-term results, in code word units, of an error detecting process in said error detecting means; a bus control means for controlling data transfer between said buffer memory, said syndrome calculating means, said error correcting means, and said error detecting means; and a system control means for performing various processes for error correction in predetermined procedures a necessary number of times, wherein

said bus control means comprises:

a before-syndrome data transfer sub means for transferring data to be corrected from said buffer memory to said syndrome calculating means and to said error detecting means concurrently in code word units until said syndrome calculating means detects an error-containing code;

an after-syndrome data transfer sub means for, when said syndrome calculating means detects an error-containing code, transferring subsequent data in said buffer memory only to said syndrome calculating

means in code word units; and

an error-detecting data transfer sub means for, after said error correcting means corrects an error contained in data in said buffer memory based on the syndrome transmitted by said syndrome calculating means, transferring error-corrected data which include the code word from which the error-containing code has been detected up to and including a final code word from said buffer memory to said error detecting means in code word units for error detection;

said error detecting means comprises:

a parallel process sub means for, until said syndrome calculating means detects an error-containing code, storing the mid-term results of the error detecting process to said storing means in code word units, and executing error detection of a code word transmitted from said buffer memory in parallel with syndrome calculation done by said syndrome calculating means; and

an after-correction error detecting sub means for, after said syndrome calculating means detects an error-containing code, executing error detection for data transferred from said buffer memory after the error correction done by said error correcting means, following a code word which has previous contents before the occurrence of an error and which is already stored in said storing means.

2. The error detection device of claim 1 further comprising a DMA control means for controlling DMA transfer to said buffer memory, wherein

said system control means comprises:

a first DMA transfer sub means for providing said DMA control means with a first DMA transfer instruction indicating that data to be corrected should be transferred from said buffer memory to said syndrome calculating means and to said error detecting means at the start of an error correcting process; and

a second DMA transfer sub means for, after having been informed of completion of error correction by said error correcting means, only when said syndrome calculating means has detected an error-containing code, providing said DMA control means with a second DMA transfer instruction indicating that subsequent data including a code word from which said error-containing code has been detected based on error-containing code word information transmitted by said syndrome calculating means should be transferred from said buffer memory to said error detecting means; and

said DMA control means comprises:

a transfer control sub means for making a request of said bus control means to perform DMA transfer in accordance with the first DMA transfer instruction and the second DMA transfer instruction transmitted by said system control means.

3. An error correction device comprising: a buffer memory for storing at least one sector of data having a structure where each of N words of error correcting code comprises a data unit, an inner code parity unit, and one error detecting code; a syndrome calculating means for generating syndrome for data read from said buffer memory; an error correcting means for correcting error-containing data in said buffer memory by

detecting an error position from the syndrome generated by said syndrome calculating means and by calculating an error value; an error detecting means for detecting an error, one sector at a time, in error-corrected data generated by said error correcting means; a bus control means for controlling data transfer between said buffer memory, said syndrome calculating means, said error correcting means, and said error detecting means; and a system control means for performing various processes for error correction in predetermined procedures a necessary number of times; wherein

said bus control means comprises:

a concurrent data transfer sub means for transferring data to be corrected from said buffer memory to said syndrome calculating means and to said error detecting means concurrently in code word units until said syndrome calculating means detects an error-containing code; and

an error-detecting data transfer sub means for, only when said syndrome calculating means has detected an error-containing code, after the error correction done by said error correcting means, transferring data in a sector containing_error-corrected data in and after the code word from which the error-containing code has been detected, from said buffer memory to said error detecting means for error detection,

said error detecting means comprises:

a parallel error detecting sub means for executing error detection for a code word transmitted from said buffer memory, in parallel with the syndrome calculation done by said syndrome calculating means; and

an error re-detecting sub means for, only when said syndrome

calculating means has detected an error-correcting code, executing error detection one more time for the error-corrected data.

4. The error correction device of claim 3 further comprising a DMA control means for controlling DMA transfer to said buffer memory, wherein said system control means comprises:

a first DMA transfer sub means for providing said DMA control means with a first DMA transfer instruction indicating that data to be corrected should be transferred from said buffer memory to said syndrome calculating means and to said error detecting means at the start of an error correcting process; and

a second DMA transfer sub means for, after having been informed of completion of error correction by said error correcting means, only when said syndrome calculating means has detected an error-containing code, providing said DMA control means with a second DMA transfer instruction indicating that a sector containing the data from which said error-containing code has been detected should be transferred from said buffer memory to said error detecting means; and

said DMA control means comprises:

a transfer control sub means for making a request of said bus control means to perform DMA transfer in accordance with the first DMA transfer instruction and the second DMA transfer instruction transmitted by said system control means.

5. An error correction device comprising: a buffer memory for

storing at least one sector of data having a structure where each of N words of error correcting code comprises a data unit, an inner code parity unit, and one error detecting code; a syndrome calculating means for generating syndrome for data read from said buffer memory; an error correcting means for correcting error-containing data in said buffer memory by detecting an error position from the syndrome generated by said syndrome calculating means and by calculating an error value; an error detecting means for detecting an error, one sector at a time, in error-corrected data generated by said error correcting means; a storing means for storing mid-term results, in code word units, of an error detecting process in said error detecting means; a bus control means for controlling data transfer between said buffer memory, said syndrome calculating means, said error correcting means, and said error detecting means; and a system control means for performing various processes for error correction in predetermined procedures a necessary number of times, wherein

said bus control means comprises:

a first transfer sub means for executing a first transfer where data to be corrected are transferred in code word units from said buffer memory concurrently to said syndrome calculating means and to said error detecting means until said syndrome calculating means detects an error-containing code, and for suspending the first transfer when said syndrome calculating means has detected an error-containing code; and

a second transfer sub means for executing a second transfer where a code word from which an error has been detected and corrected is transferred from said buffer memory to said error detecting means after

the error correction done by said error correcting means, based on the syndrome transmitted from said syndrome calculating means; and

a first transfer resuming sub means for, after the completion of the second transfer, making the first transfer sub means resume the first transfer for subsequent code words including the code word which has been subjected to the second transfer, and

said error detecting means comprises:

a first error detecting sub means for, until said syndrome calculating means detects an error-containing code, executing a first error detection where error detection is performed for a code word transmitted from said buffer memory in parallel with the syndrome calculation done by said syndrome calculating means, while storing mid-term results of the error detection in code word units to said storing means;

a second error detecting sub means for, after said syndrome calculating means detects an error-containing code, executing a second error detection where error detection is resumed for code words whose errors have been detected and corrected by said error correcting means, starting at a code word which has previous contents before the occurrence of an error and which is already stored in said storing means; and

a first error detection resuming sub means for, after the completion of the second error detection for the error-corrected code word, making the first error detecting sub means resume the first error detection for subsequent code words.

6. The error correction device of claim 5 further comprising a DMA

control means for controlling DMA transfer to said buffer memory, wherein said system control means comprises:

a DMA transfer instruction sub means for providing said DMA control means with a DMA transfer instruction indicating that data to be corrected should be transferred from said buffer memory to said syndrome calculating means and to said error detecting means at the start of an error correcting process; and

said DMA control means comprises a data transfer control sub means for making a request of said bus control means to perform DMA transfer in accordance with the DMA transfer instruction transmitted by said system control means.

7. An error correction device comprising; a buffer memory for storing at least one ECC block of data having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to error correction; a syndrome calculating means for generating syndrome for data read from said buffer memory; an error correcting means for correcting error-containing data in said buffer memory by detecting an error position from the syndrome generated by said syndrome calculating means and by calculating an error value; an error detecting means for detecting an error in error-corrected

data generated by said error correcting means; a bus control means for controlling data transfer between said buffer memory, said syndrome calculating means, said error correcting means, and said error detecting means; and a system control means for performing various processes for error correction in predetermined procedures a necessary number of times, wherein

said system control means comprises:

a first-time error correction sub means for reading data from said buffer memory in a same direction as calculation for an error detecting code as a first-time error correction; for transferring the read data to said syndrome calculating means and to said error detecting means concurrently until said syndrome calculating means detects an error-containing code; for making said syndrome calculating means execute syndrome calculation and said error detecting means execute error detection in parallel; for making said error correcting means execute error correction when said syndrome calculating means has detected an error-containing code; and for making one of said syndrome calculating means and said error correcting means provide the system control means with information which designates a code word containing the error-containing code;

an even-numbered error correction sub means for reading a code word in a different direction from a preceding odd-numbered error correction; for transferring the code word to said syndrome calculating means and to said error detecting means concurrently until said syndrome calculating means detects an error-containing code; for making said syndrome calculating

means execute syndrome calculation and said error detecting means execute error detection in parallel; for making said error correcting means execute error correction when said syndrome calculating means detects an error-containing code; and for making said error correcting means provide said system control means with information which designates the position of the error-containing code in an error correcting code word obtained in the error correction;

a non-error range designating sub means for designating, one sector at a time, a range from which an error-containing code has not been detected at the odd-numbered error correction or the subsequent even-numbered error correction, based on said information that designates the code word including the error-containing code and said information that designates the position of the error-containing code in the error correcting code word;

an odd-numbered error correction sub means for, as an odd-numbered error correction as a third-time or later error correction, providing concurrently said syndrome calculating means and said error detecting means with a code in the same direction as in the previous odd-numbered error correction except for a sector in one ECC block which has been designated by said non-error range designating sub means as the range from which an error-containing code has not been detected in and before the preceding even-numbered error correction until said syndrome calculating means detects an error-containing code; for making said syndrome calculating means execute syndrome calculation and said error detecting means execute error detection in parallel; for making said error

correcting means execute error correction when said syndrome calculating means detects an error-containing code; and for making one of said syndrome calculating means and said error correcting means provide said system control means with information which designates the code word including the error-containing code; and

a number-of-times control sub means for repeating the odd-numbered error correction and the even-numbered error correction a predetermined number of times.

8. The error correction device of claim 7, wherein said number-of-times control sub means is a three-time repetition control sub means for repeating the error correction three times at most.

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9. The error correction device of claim 7 or 8 further comprising a storing means for storing mid-term results, in code word units, of each code word from which no error has been detected in the error detecting process done by said error detecting means until said syndrome calculating means detects an error-containing code, wherein

said non-error range designating sub means is a non-error sector code word range designating sub means for designating, in code word units of a sector, a range from which an error-containing code has not been detected in the odd-numbered error correction or the subsequent even-numbered error correction, based on said information that designates the code word including the error-containing code and on said information that designates the position of the error-containing code in the error correcting code word;

and

said odd-numbered error correction sub means is an odd-numbered error correction sub means with mid-term results for, in the third-time or later odd-numbered error correction, making said bus control means start a concurrent data transfer not at the head but at the code word of the sector from which an error-containing code has been detected, based on the information designated by said non-error sector code word range designating sub means; for making said syndrome calculating means start syndrome calculation at the code word; and for making said error detecting means start error detection at a code word somewhere in the middle of the sector by using contents stored in said storing means as an initial value.

10. The error correction device of claim 7 or 8 further comprising a sector-basis storing means for storing mid-term results, on a sector-by-sector basis, in code word units, of each code word from which no error has been detected in the error detecting process done by said error detecting means, until said syndrome calculating means detects an error-containing code, wherein

said non-error range designating sub means is a sector-basis non-error code word range designating sub means for designating, on a sector-by-sector basis, in code word units, a range from which an error-containing code has not been detected in the odd-numbered error correction or the subsequent even-numbered error correction, based on said information that designates the code word including the error-containing code and on said information that designates the position of the

error-containing code in the error correcting code word; and

said odd-numbered error correction sub means is an odd-numbered error correction sub means with mid-term results for, in the third-time or later odd-numbered error correction, making said bus control means start a concurrent data transfer not at the head but at the code word of each sector from which an error-containing code has been detected, based on the information designated by said sector-basis non-error code word range designating sub means; for making said syndrome calculating means start syndrome calculation at the code word; and for making said error detecting means start error detection at a code word somewhere in the middle of the sector by using contents stored in said sector-basis storing means as an initial value.

11. The error correction device of claim 7 or 8 further comprising a sector-group-basis storing means for storing mid-term results, on a sector-group-by-sector-group-basis, in code word units, of each code word from which no error has been detected in the error detecting process done by said error detecting means until said syndrome calculating means detects an error-containing code, wherein

said non-error range designating sub means is a sector-group-basis non-error code word range designating sub means for designating, on a sector-group-by-sector-group-basis, in code word units, a range from which an error-containing code has not been detected in the odd-numbered error correction or the subsequent even-numbered error correction, based on said information that designates the code word including the error-containing

code and on said information that designates the position of the error-containing code in the error correcting code word; and

said odd-numbered error correction sub means is an odd-numbered error correction sub means with mid-term results for, in the third-time or later odd-numbered error correction, making said bus control means start a concurrent data transfer not at the head but at the code word of each sector group from which an error-containing code has been detected, based on the information designated by said sector-group-basis non-error code word range designating sub means; for making said syndrome calculating means start syndrome calculation at the code word; and for making said error detecting means start error detection at a code word somewhere in the middle of the sector by using contents stored in said sector-group-basis storing means as an initial value.

12. The error correction device of claim 1, 2, 5, 6, 7, or 8, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-division storing means for storing said plurality of ECC blocks on a block-by-block basis;

said system control means comprises:

a means-basis ECC block pipeline processing notification sub means for transmitting ECC blocks which have been subjected to error correction downstream; for storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a means-basis ECC block recognition sub means for recognizing a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; for recognizing the error correction done by said error correcting means; for recognizing writing of error-corrected data to said plural-ECC-block-division buffer memory done by said bus control means; for recognizing an ECC block in process when said error detecting means stores mid-term results to said plural-ECC-block-division storing means, and for selecting ECC blocks to be processed; and

an ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said

DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

13. The error correction device of claim 9, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-division storing means for storing said plurality of ECC blocks on a block-by-block basis;

said system control means comprises:

a means-basis ECC block pipeline processing notification sub means for transmitting ECC blocks which have been subjected to error correction

downstream; for storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a means-basis ECC block recognition sub means for recognizing a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; for recognizing the error correction done by said error correcting means; for recognizing writing of error-corrected data to said plural-ECC-block-division buffer memory done by said bus control means; for recognizing an ECC block in process when said error detecting means stores mid-term results to said plural-ECC-block-division storing means, and for selecting ECC blocks to be processed; and

an ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

14. The error correction device of claim 10, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-division storing means for storing said plurality of ECC blocks on a block-by-block basis;

said system control means comprises:

a means-basis ECC block pipeline processing notification sub means for transmitting ECC blocks which have been subjected to error correction downstream; for storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a means-basis ECC block recognition sub means for recognizing a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means

for error detection and error correction; for recognizing the error correction done by said error correcting means; for recognizing writing of error-corrected data to said plural-ECC-block-division buffer memory done by said bus control means; for recognizing an ECC block in process when said error detecting means stores mid-term results to said plural-ECC-block-division storing means, and for selecting ECC blocks to be processed; and

an ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

15. The error correction device of claim 11, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction

(data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-division storing means for storing said plurality of ECC blocks on a block-by-block basis;

said system control means comprises:

a means-basis ECC block pipeline processing notification sub means for transmitting ECC blocks which have been subjected to error correction downstream; for storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a means-basis ECC block recognition sub means for recognizing a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; for recognizing the error correction done by said error correcting means; for recognizing writing of error-corrected data to said plural-ECC-block-division buffer memory done by said bus control means; for recognizing an ECC block in process when said error detecting means stores mid-term results to said plural-ECC-block-division storing means, and for selecting ECC blocks to be processed; and

an ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

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16. The error correction device of claim 1, 2, 5, 6, 7, or 8, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction;

said buffer memory is an ECC-block-basis buffer memory for storing, on a block-by-block basis, ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-and-code word-division storing means for storing ECC blocks in process on a

block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis;

said system control means comprises:

an means-basis ECC block pipeline processing notification sub means for transmitting ECC blocks which have been subjected to error correction downstream; for storing ECC blocks to be processed next to said ECC-block-basis buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a means-basis ECC block code word recognition sub means for selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; in controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means by said error detecting means; and

an ECC block code word recognition sub means in sub means-basis pipeline processing for making said first error detecting sub means, said even-numbered error correction sub means, said even-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means in said system control means

recognize that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said ECC-block-basis buffer memory, and further making these same sub means contained in said system control means recognize the ECC blocks and the code words which are to be processed therein.

17. The error correction device of claim 9, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction;

said buffer memory is an ECC-block-basis buffer memory for storing, on a block-by-block basis, ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-and-code word-division storing means for storing ECC blocks in process on a block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis;

said system control means comprises:

an means-basis ECC block pipeline processing notification sub means for transmitting ECC blocks which have been subjected to error correction

downstream; for storing ECC blocks to be processed next to said ECC-block-basis buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a means-basis ECC block code word recognition sub means for selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; in controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means by said error detecting means; and

an ECC block code word recognition sub means in sub means-basis pipeline processing for making said first error detecting sub means, said even-numbered error correction sub means, said even-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means in said system control means recognize that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said ECC-block-basis buffer memory, and further making these same sub means contained in said system control means recognize the ECC blocks and the code words which are to be processed therein.

18. The error correction device of claim 10, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction;

said buffer memory is an ECC-block-basis buffer memory for storing, on a block-by-block basis, ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-and-code word-division storing means for storing ECC blocks in process on a block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis;

said system control means comprises:

an means-basis ECC block pipeline processing notification sub means for transmitting ECC blocks which have been subjected to error correction downstream; for storing ECC blocks to be processed next to said ECC-block-basis buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a means-basis ECC block code word recognition sub means for

selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; in controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means by said error detecting means; and

an ECC block code word recognition sub means in sub means-basis pipeline processing for making said first error detecting sub means, said even-numbered error correction sub means, said even-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means in said system control means recognize that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said ECC-block-basis buffer memory, and further making these same sub means contained in said system control means recognize the ECC blocks and the code words which are to be processed therein.

19. The error correction device of claim 11, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and

horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction;

said buffer memory is an ECC-block-basis buffer memory for storing, on a block-by-block basis, ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-and-code word-division storing means for storing ECC blocks in process on a block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis;

said system control means comprises:

an means-basis ECC block pipeline processing notification sub means for transmitting ECC blocks which have been subjected to error correction downstream; for storing ECC blocks to be processed next to said ECC-block-basis buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a means-basis ECC block code word recognition sub means for selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; in

controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means by said error detecting means;

an ECC block code word recognition sub means in sub means-basis pipeline processing for making said first error detecting sub means, said even-numbered error correction sub means, said even-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means in said system control means recognize that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said ECC-block-basis buffer memory, and further making these same sub means contained in said system control means recognize the ECC blocks and the code words which are to be processed therein.

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20. The error correction device of claim 1, 2, 5, 6, 7, or 8 wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-division storing means for storing said plurality of ECC blocks on a block-by-block basis;

said system control means comprises:

a collective-type means-basis ECC block pipeline processing notification sub means for collectively transmitting ECC blocks which have been subjected to error correction downstream; for collectively storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a collective-type means-basis ECC block recognition sub means for recognizing a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; for recognizing the error correction done by said error correcting means; for recognizing writing of error-corrected data to said plural-ECC-block-division buffer memory by said bus control means; for recognizing ECC blocks in process when said error detecting means stores mid-term results to said plural-ECC-block-division storing means, and for selecting ECC blocks to be processed; and

a collective-type ECC block notification sub means in sub means-basis

pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively transmitted downstream and new ECC blocks to be processed have been collectively stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

21. The error correction device of claim 9 wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-division storing means for storing said plurality of ECC blocks on a block-by-block basis;

said system control means comprises:

a collective-type means-basis ECC block pipeline processing notification sub means for collectively transmitting ECC blocks which have been subjected to error correction downstream; for collectively storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a collective-type means-basis ECC block recognition sub means for recognizing a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; for recognizing the error correction done by said error correcting means; for recognizing writing of error-corrected data to said plural-ECC-block-division buffer memory by said bus control means; for recognizing ECC blocks in process when said error detecting means stores mid-term results to said plural-ECC-block-division storing means, and for selecting ECC blocks to be processed; and

a collective-type ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively transmitted downstream and new ECC blocks to be processed have been

collectively stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

22. The error correction device of claim 10, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-division storing means for storing said plurality of ECC blocks on a block-by-block basis;

said system control means comprises:

a collective-type means-basis ECC block pipeline processing notification sub means for collectively transmitting ECC blocks which have been subjected to error correction downstream; for collectively storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said

syndrome calculating means, said error detecting means, and said error correcting means;

a collective-type means-basis ECC block recognition sub means for recognizing a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; for recognizing the error correction done by said error correcting means; for recognizing writing of error-corrected data to said plural-ECC-block-division buffer memory by said bus control means; for recognizing ECC blocks in process when said error detecting means stores mid-term results to said plural-ECC-block-division storing means, and for selecting ECC blocks to be processed; and

a collective-type ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively transmitted downstream and new ECC blocks to be processed have been collectively stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

23. The error correction device of claim 11, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a

structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-division storing means for storing said plurality of ECC blocks on a block-by-block basis;

said system control means comprises:

a collective-type means-basis ECC block pipeline processing notification sub means for collectively transmitting ECC blocks which have been subjected to error correction downstream; for collectively storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a collective-type means-basis ECC block recognition sub means for recognizing a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; for recognizing

the error correction done by said error correcting means; for recognizing writing of error-corrected data to said plural-ECC-block-division buffer memory by said bus control means; for recognizing ECC blocks in process when said error detecting means stores mid-term results to said plural-ECC-block-division storing means, and for selecting ECC blocks to be processed; and

a collective-type ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively transmitted downstream and new ECC blocks to be processed have been collectively stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

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24. The error correction device of claim 1, 2, 5, 6, 7, or 8, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as

sector) as a unit are subjected to the error correction;

said buffer memory is an ECC-block-basis buffer memory for storing, on a block-by-block basis, ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-and-code word-division storing means for storing ECC blocks in process on a block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis;

said system control means comprises:

a collective-type means-basis ECC block pipeline processing notification sub means for collectively transmitting ECC blocks which have been subjected to error correction downstream; for collectively storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a collective-type means-basis ECC block code word recognition sub means for selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; in controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing

mid-term results to said ECC-block-and-code word-division storing means by said error detecting means; and

a collective-type ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively transmitted downstream and new ECC blocks to be processed have been collectively stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

25. The error correction device of claim 9, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction;

said buffer memory is an ECC-block-basis buffer memory for storing, on a block-by-block basis, ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting

process generated by said error detecting means is an ECC-block-and-code word-division storing means for storing ECC blocks in process on a block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis;

said system control means comprises:

a collective-type means-basis ECC block pipeline processing notification sub means for collectively transmitting ECC blocks which have been subjected to error correction downstream; for collectively storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a collective-type means-basis ECC block code word recognition sub means for selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; in controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means by said error detecting means; and

a collective-type ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said

even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively transmitted downstream and new ECC blocks to be processed have been collectively stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

26. The error correction device of claim 10, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction;

said buffer memory is an ECC-block-basis buffer memory for storing, on a block-by-block basis, ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-and-code word-division storing means for storing ECC blocks in process on a block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis;

said system control means comprises:

a collective-type means-basis ECC block pipeline processing notification sub means for collectively transmitting ECC blocks which have been subjected to error correction downstream; for collectively storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a collective-type means-basis ECC block code word recognition sub means for selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; in controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means by said error detecting means; and

a collective-type ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively

transmitted downstream and new ECC blocks to be processed have been collectively stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

27. The error correction device of claim 11, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction;

said buffer memory is an ECC-block-basis buffer memory for storing, on a block-by-block basis, ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-and-code word-division storing means for storing ECC blocks in process on a block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis;

said system control means comprises:

a collective-type means-basis ECC block pipeline processing notification sub means for collectively transmitting ECC blocks which have been subjected to error correction downstream; for collectively storing ECC

blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a collective-type means-basis ECC block code word recognition sub means for selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; in controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means by said error detecting means; and

a collective-type ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively transmitted downstream and new ECC blocks to be processed have been collectively stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

28. An error correction device which performs error correction for data in ECC blocks each having a structure where error correcting code words each comprising a data unit and a parity unit are arranged in vertical and horizontal directions so as to realize repeated error correction, and predetermined data composed of a predetermined number of code words in the vertical or horizontal direction (data in the horizontal direction are referred to as sector) are as one unit subjected to error correction, and which also perform syndrome calculation and error detection in parallel with a storage of demodulated codes in a buffer memory, said error correction device comprising:

a first syndrome calculating means for performing syndrome calculation with said buffer memory;

a first error detecting means which pairs up with the first syndrome calculating means;

a second syndrome calculating means for performing syndrome calculation of demodulated codes without said buffer memory;

a second error detecting means which pairs up with the second syndrome calculating means;

a storing means for storing mid-term results of calculations of the first error detecting means and the second error detecting means;

a buffer memory parallel transfer means for transferring data transmitted from upstream to the second syndrome calculating means and to the second error detecting means in parallel with storage of the data in said buffer memory until the second syndrome calculating means detects

an error-containing code;

an error-detecting-means switch means for switching between the first error detection means and the second error detection means in a manner that after the second syndrome calculating means detects an error-containing code, said storing means is provided with the mid-term results of the calculation by the second error detecting means of code words until said error-containing code is detected, and on and after the second-time error correction in a same direction, after the second syndrome calculating means detects an error-containing code, said storing means is provided with the mid-term results of the calculation by the second error detecting means of code words until said error-containing code is detected;

an error correcting means for performing error correction after one of the first error detecting means and the second error detecting means detects an error-containing code word;

a parallel transfer means for, on and after the second-time error correction in the same direction, before the first syndrome calculating means detects an error-containing code, transferring data stored in said buffer memory, starting at a code word which is not stored in said storing means to the first syndrome calculating means and to the first error detecting means; and

a second-time onward detecting-processed data use means for, on and after the second-time error detection in the same direction done by the second error detecting means, performing error detection of the subsequent code words by using the mid-term results stored in said storing means.

29. An error correction device which performs error correction for data in ECC blocks each having a structure where error correcting code words each comprising a data unit and a parity unit are arranged in vertical and horizontal directions so as to realize repeated error correction, and predetermined data composed of a predetermined number of strings in the vertical or horizontal direction (data in the horizontal direction are referred to as sector) are as one unit subjected to error correction, and which also perform syndrome calculation and error detection in parallel with a storage of demodulated codes in a buffer memory, said error correction device comprising:

a first syndrome calculating means for performing syndrome calculation with said buffer memory;

a first error detecting means which pairs up with the first syndrome calculating means;

a second syndrome calculating means for performing syndrome calculation of demodulated codes without said buffer memory;

a second error detecting means which pairs up with the second syndrome calculating means;

a storing means for storing mid-term results of calculations of the first error detecting means and the second error detecting means in predetermined data units such as ECC block units, sector units, and sector group units;

a buffer memory parallel transfer means for transferring data transmitted from upstream to the second syndrome calculating means and to the second error detecting means in said data units in parallel with

storage of the data in said buffer memory until the second syndrome calculating means detects an error-containing code;

an error-detecting-means switch means for switching between the first error detection means and the second error detection means in said data units in a manner that after the second syndrome calculating means detects an error-containing code, said storing means is provided with the mid-term results of the calculation by the second error detecting means of code words until said error-containing code is detected, and on and after the second-time error correction in a same direction, after the second syndrome calculating means detects an error-containing code, said storing means is provided with the mid-term results of the calculation by the second error detecting means of code words until said error-containing code is detected;

an error correcting means for performing error correction after one of the first error detecting means and the second error detecting means detects an error-containing code word;

a parallel transfer means for, on and after the second-time error correction in the same direction, before the first syndrome calculating means detects an error-containing code, transferring data stored in said buffer memory, starting at a code word which is not stored in said storing means to the first syndrome calculating means and to the first error detecting means; and

a second-time onward detecting-processed data use means for, on and after the second-time error detection in the same direction by the second error detecting means, performing error detection of the subsequent code

words by using the mid-term results stored in said storing means.

30. An error correction device which performs error correction for data in a plurality of ECC blocks each having a structure where error correcting code words each comprising a data unit and a parity unit are arranged in vertical and horizontal directions so as to realize repeated error correction, and predetermined data composed of a predetermined number of code words in the vertical or horizontal direction (data in the horizontal direction are referred to as sector) are as one unit subjected to concurrent or parallel error correction by pipeline processing, and which also perform syndrome calculation and error detection in parallel with a storage of demodulated codes in a buffer memory, said error correction device comprising:

a buffer memory for storing ECC blocks to be processed in pipeline, on a block-by-block basis;

a first syndrome calculating means for performing syndrome calculation;

a first error detecting means which pairs up with the first syndrome calculating means;

a second syndrome calculating means for performing syndrome calculation;

a storing means for storing the mid-term results of the calculation done by the first error detecting means and the second error detecting means in predetermined data units of the ECC blocks in process such as ECC block units, sector units, or sector group units;

a demodulated-code calculation selecting means for making one of the first syndrome calculating means and the second syndrome calculating means execute syndrome calculation for demodulated data transmitted from upstream, and making the other syndrome calculating means execute syndrome calculation when there are data stored in said buffer memory;

a buffer memory parallel transfer means for, before the syndrome calculating means selected by said demodulated-code calculation selecting means detects an error-containing code, sequentially transferring data from upstream to the syndrome calculating means and the error detecting means which pairs up therewith, and at the same time storing the data in said buffer memory;

an error-detecting-means switch means for switching between the first error detection means and the second error detection means in a manner that after the syndrome calculating means selected by said demodulated-code calculation selecting means detects an error-containing code in data transmitted from upstream in said data units, said storing means is provided with the mid-term results of the calculation by the corresponding error detecting means of code words until said error-containing code is detected, and on and after the second-time error correction in a same direction, after the corresponding second syndrome calculating means detects an error-containing code, said storing means is provided with the mid-term results of the calculation by the corresponding error detecting means of code words until said error-containing code is detected;

an error correcting means for performing error correction after the

first error detecting means or the second error detecting means detects an error-containing code word;

a stored code calculation selecting means for selecting between the first syndrome calculating means and the second syndrome calculating means in ECC block units or in said data units so as to perform syndrome calculation for the data stored in said buffer memory;

a parallel transfer means for, on and after the second-time error correction in a same direction, before the first syndrome calculating means detects an error-containing code in said data units, transferring code words not stored in said storing means out of data stored in said buffer memory to the corresponding one of the first syndrome calculating means and the first error detecting means;

a second-time onward detecting-processed data use means for, on and after the second-time error detection in the same direction done by the corresponding error detecting means, performing error detection of the subsequent code words in said data units by using the mid-term results stored in said storing means;

a means-basis pipeline processing notification means for transmitting ECC blocks which have been subjected to error correction downstream; for storing ECC blocks to be processed next to said buffer memory; and for making the storage known to said stored code calculation selecting means, said buffer memory parallel transfer means, said error-detecting-means switch means, the first syndrome calculating means, the second syndrome calculating means, said error detecting means, said error correcting means, said parallel transfer means, and said second-time onward

detecting-processed data use means; and

a system control means for controlling a data transfer and data rewriting of ECC blocks in process in ECC block units or said data units at each means and for coordinating with other means the transfer of error-corrected ECC blocks downstream and the storage of new ECC blocks to be processed in said buffer memory.

31. The error correction device of claim 1, 2, 3, 4, 5, 6, 7, 8, 28, 29, or 30 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

32. The error correction device of claim 9 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction

and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

33. The error correction device of claim 10 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

34. The error correction device of claim 11 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error

correction alternately in units of said predetermined capacity.

35. The error correction device of claim 12 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

36. The error correction device of claim 13 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

37. The error correction device of claim 14 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

38. The error correction device of claim 15 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

39. The error correction device of claim 16 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two

buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

40. The error correction device of claim 17 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

41. The error correction device of claim 18 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

42. The error correction device of claim 19 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

43. The error correction device of claim 20 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

44. The error correction device of claim 21 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

45. The error correction device of claim 22 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

46. The error correction device of claim 23 further comprising:

two buffer memories each having a predetermined capacity

equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

47. The error correction device of claim 24 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

48. The error correction device of claim 25 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous

data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

49. The error correction device of claim 26 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

50. The error correction device of claim 27 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said

two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.